IMPATT Diode Circuit Design for Parametric Stability

JOSEPH GONDA AND WILLIAM E. SCHROEDER, MEMBER, IEEE

Abstract—**A new approach to IMPATT diode circuit design to achieve freedom from parametric instabilities is described. Necessary and sufficient conditions are described in the frequency domain for the load impedance presented to the diode terminals. A number of unconditionally stable circuits have been developed for flat-profile GaAs diodes using this approach. Three of these circuits have been built and tested experimentally in 11-GHz IMPATT oscillators and amplifiers. These experimental circuits have been free of parametric instability, even when driven into full RF saturation. In a systems application practical constraints such as cost, RF loss, and tunability will require compromises which will degrade the stability, and it may not always be possible to achieve complete stability for a given diode.**

I. INTRODUCTION

IMPATT DIODES exhibit negative resistance in a wide frequency range, usually approaching an octave. Proper load impedance design within this frequency range, i.e., providing low resistance at the desired operating frequency and high resistance over the rest of the band, yields oscillator and amplifier circuits which work sufficiently well for small-signal levels.

At large RF levels, however, these circuits often produce "secondary effects" such as

a) spurious tones;
b) excessive noise;
c) premature saturation of output power;
d) low efficiency;
e) impaired frequency stability in free-running oscillators;
f) diode burnout.

These effects seriously limit circuit performance.

Several of these "secondary effects" have been described previously. Brackett [1] gave an explanation for low-frequency (bias-circuit) instabilities. He showed that the source of these instabilities and associated bias-circuit oscillations is a low-frequency negative resistance, induced by the rectification properties of the nonlinear microwave avalanche under large-signal conditions.

Hines [2] presented a theory for parametric instabilities in IMPATT diode circuits, which is based on the nonlinear inductive behavior of the avalanche process (somewhat analogous to the nonlinear capacitance effect in varactor diodes), under large-signal conditions.

It is apparent from these works that the presence of a large-amplitude "pump" signal is always required to produce the instabilities. This pump signal can be the amplified external signal in the case of an amplifier or the free-running oscillation signal in the case of an oscillator. It is also apparent that the impedance characteristics of the load presented to the diode, far from the operating frequency and even far outside the negative resistance region of the diode, have a profound effect on stability. For stable operation, the load impedance should be well controlled from dc up to above the operating frequency.

Using Hines' model Schroeder [3] developed criteria to test IMPATT diode circuits for parametric stability. These criteria will be reviewed here and will be used throughout this paper. Design criteria for the external impedance presented to the diode wafer to prevent parametric instabilities were also developed. These criteria are sufficient, but not necessary, to achieve stable operation.

Another model for parametric instabilities, similar in approach to that of Hines, has been described by Goedbloed and Tjassens [4] and Goedbloed [5]. They verified the theory experimentally and observed that reducing the diode capacitance increases the parametric stability, a result also noted in [3]. They did not, however, apply the theory to the design of stable circuits.

A special case of parametric instability, the degenerate one where there is a single tone at one half the pump signal frequency, has been studied extensively by Peterson [6]. He identified the admittance region which the circuit must avoid at the subharmonic frequency in order to be stable for all pump levels. While Peterson's results can be used to design a circuit which is stable at the subharmonic frequency, they are not sufficient to insure general parametric stability.

It has been our experience that circuits designed considering only the subharmonic impedance requirement very often develop a parametrically related pair of tones when strongly pumped. Thus the general parametric case should be considered from the start of the circuit design.

This paper provides a method to achieve freedom from parametric instabilities. It is applicable to all types of IMPATT amplifiers and oscillators. Necessary and sufficient conditions are derived for the load impedance presented to the terminals of the encapsulated diode. Stability diagrams are given which enable the designer to see graphically the circuit impedance behavior required. Examples of stable amplifier and oscillator designs are described in detail. Three of these circuits have been built and tested in the laboratory. No sudden noise increase, spurious tones, or premature power saturation were found even when the diodes were driven into full RF saturation.

In some applications parametrically generated tones may be desirable. For example, a frequency divider can be made by pumping an IMPATT diode and extracting the nth sub-

Manuscript received July 6, 1976; revised November 8, 1976.
J. Gonda is with Bell Labs., Inc., North Andover, MA 01845.
W. E. Schroeder is with Bell Labs., Inc., Allentown, PA 18103.

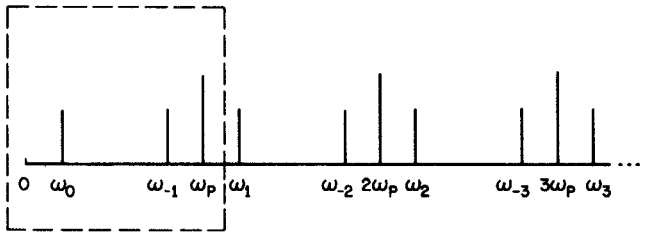

Fig. 1. Signal spectrum in an IMPATT diode circuit, strongly pumped at ω_p and excited by a weak signal at ω_0 simultaneously.

harmonic. Although this paper is directed toward suppressing parametric tones, the theory could also be useful in designing circuits which deliberately generate such tones.

II. Review of the Criteria for Parametric Stability

Due to the nonlinear inductive reactance effect in the semiconductor avalanche, strongly driven IMPATT diodes can generate negative resistance at almost any frequency. The stability of such a system pumped at ω_p can be analyzed by perturbing it with a weak signal at some other frequency ω_0. The multifrequency response of the system, shown in Fig. 1, can then be examined and the conditions for stability found [2]. In the general form, these conditions are too complicated to give guidance for practical circuit design.

In our experience spurious oscillations in the frequency range $\omega_0 \ll \omega_p/2$ do not occur when Brackett's criterion is satisfied. Parametric instabilities usually occur in the frequency range $(\omega_p/4) \lesssim \omega_0 \leq (\omega_p/2)$. In this range it is a good approximation, as suggested previously [3], to simplify the multifrequency interaction to a single parametric pair, ω_0 and ω_{-1}. These frequencies are interrelated through the pump frequency as

$$\omega_p = \omega_0 + \omega_{-1}. \tag{1}$$

A complex quantity, called the stability factor, can be associated with the spectral components at ω_0 and ω_{-1}. These stability factors are defined by the following expression:

$$S_n = S(\omega_n) = 1 + \left(\frac{\omega_n^2}{\omega_a^2 - \omega_n^2}\right) \frac{Z_X(\omega_n) + (1/j\omega_n C_T)}{Z_X(\omega_n) + Z_W(\omega_n)}, \qquad n = 0, -1 \tag{2}$$

where

ω_a small-signal avalanche frequency of the diode;
C_T diode junction capacitance at breakdown at the operating temperature;
Z_X external impedance, presented to the diode wafer;

and

$$Z_W(\omega) = \frac{\bar{x}_d(1 - (\sin\theta_d/\theta_d)) - \omega^2/\omega_a^2 + j\bar{x}_d((1 - \cos\theta_d)/\theta_d)}{j\omega C_T(1 - (\omega^2/\omega_a^2))} \tag{3}$$

is the small-signal Read model impedance of the diode wafer, where

$\bar{x}_d$ ratio of drift length to total length of diode;
$\theta_d = \omega\tau_d$ transit angle of the drift region.

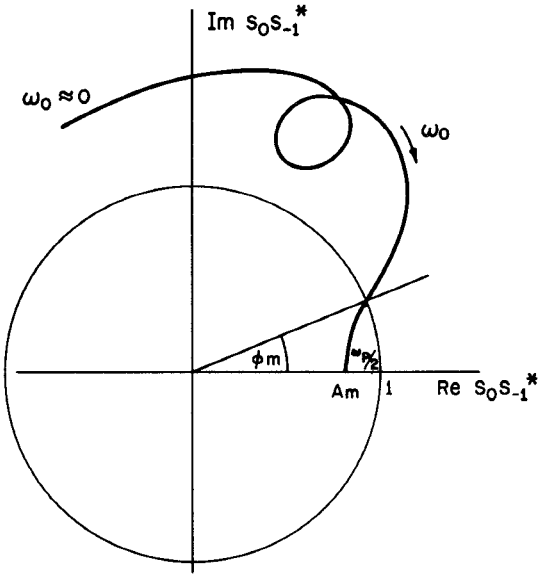

Fig. 2. The stability curve $S_0 S^*_{-1}(\omega_0)$ on the complex plane.

The condition for the threshold of parametric instability is

$$|M_1|^2 S_0 S^*_{-1} = 1, \qquad M_1 = \frac{I_p}{2I_{dc}} \tag{4}$$

where

I_p avalanche particle current at the pump frequency;
I_{dc} direct current;

and the asterisk denotes complex conjugate.

The quantity M_1 varies from zero to one as the pump signal varies from the small-signal to the extreme large-signal limit. When M_1 is sufficiently small there is no parametric oscillation. Thus it is clear that if, and only if,

$$\text{Im}\,(S_0 S^*_{-1}) = 0 \quad \text{and} \quad \text{Re}\,(S_0 S^*_{-1}) > 1 \tag{5}$$

at a pair of frequencies ω_0 and ω_{-1}, will the circuit produce, for a sufficiently high pump level, parametric tones at frequencies ω_0 and ω_{-1}.

The threshold condition, equation (4), is the same as that given by Hines [2] and Goedbloed [5] for the two-frequency case. It is also identical to Peterson's criterion for the subharmonic case [6] when an infinitesimal avalanche width is assumed.

In order to test a circuit for parametric stability, the quantity $S_0 S^*_{-1}$ should be plotted for the circuit in question on a complex plane for all ω_0 frequencies from low frequencies up to $\omega_p/2$, as shown in Fig. 2. In the case of an unstable circuit when condition (5) is met at some pair of frequencies ω_0 and ω_{-1}, the stability curve will intersect the real axis above one for frequency ω_0. On the other hand, if the circuit in question is unconditionally stable, i.e., stable for all drive levels at all frequencies, its stability curve does not intersect the real axis above one.

The stability curve of Fig. 2 corresponds to such an unconditionally stable circuit. The curve shown intersects the real axis at $A_m < 1$, and the magnitude is less than one up to a phase angle of ϕ_m. Since the stability curve closely resembles the open-loop gain of a feedback amplifier, A_m and

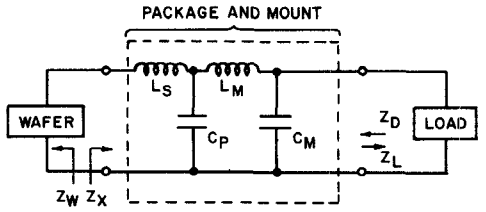

Fig. 3. Impedance transformation between the diode wafer and external load due to the package and mount parasitics.

ϕ_m can be considered measures of amplitude and phase margin, respectively, against parametric instabilities.

It should be noted that at frequency $\omega_p/2$ the stability factors S_0 and S_{-1} are identical and $S_0 S_{-1}^* = |S_0|^2$; therefore, the stability curve always ends on the real axis. For unconditional stability at the subharmonic frequency it is necessary then to satisfy the following condition:

$$|S_0(\omega_p/2)| < 1. \tag{6}$$

It is clear that a circuit is unconditionally stable if $|S| < 1$ at all frequencies from dc to f_p, but this is a necessary condition only at the subharmonic frequency. In the previous paper [3] the locus of $|S| = 1$ was mapped onto the circuit-impedance plane, so that the circuit behavior needed to give $|S| < 1$ at all frequencies was defined. For some diode cases, realizing such a circuit is difficult. In this paper the complete S plane is mapped onto the circuit-impedance plane, so that circuits which have $|S| > 1$ for some frequencies may be designed to be unconditionally stable, by controlling the phase of S. The stability curve of Fig. 2 is an example of a curve for such a circuit.

In the preceding discussion attention has been focused on *unconditional* stability. In some cases, unconditional stability may be difficult to obtain or may not be required. It is apparent from (4) that when the real-axis intercept of $S_0 S_{-1}^*$ is larger than one, the circuit is stable up to a certain value of M_1. For uniformly doped GaAs diodes, the maximum output power corresponds to $M_1 \simeq 0.8$, typically [7]. Thus a stability diagram for such a diode need only have a real-axis intercept less than $(0.8)^{-2} = 1.56$ to be stable from small signals to the point of maximum power.

III. Circuit Design

A. General Considerations

For the circuit designer the diode wafer is usually inaccessible. It is embedded in a package and mount as shown in Fig. 3, which transforms the wafer impedance $Z_W(f)$ into the diode impedance $Z_D(f)$. This impedance can be calculated if Z_W and the package and mount parasitics are known, or it can be measured directly for a given diode. For illustration, the result, in terms of $-Z_D(f)$, has been calculated and plotted on a Smith chart as shown in Fig. 4 for a GaAs diode mounted in a standard microwave package. The diode impedance is plotted in the active frequency band of the diode only, and in order to bring the curve inside the Smith chart the sign of $Z_D(f)$ has been reversed.

The task is to design a load impedance $Z_L(f)$ for the given diode. When connected to the diode terminals, this impedance should satisfy three sets of requirements simultaneously:

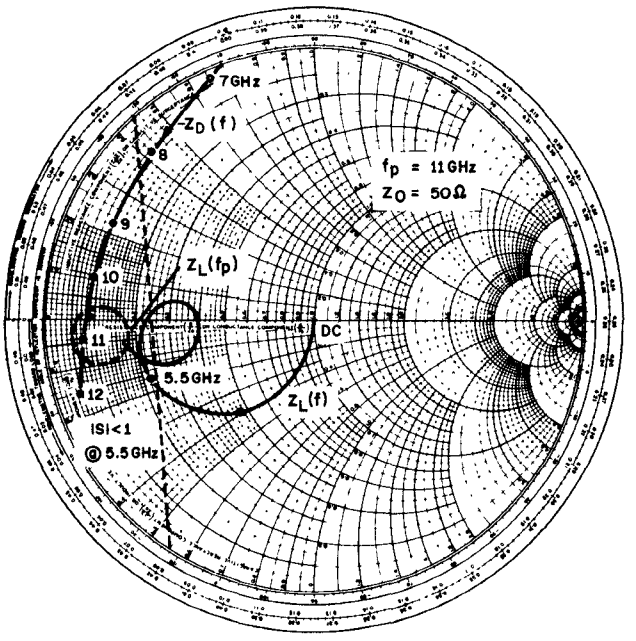

Fig. 4. Small-signal diode impedance $-Z_D(f)$ and the boundary of the stable region at 5.5 GHz. Also shown is a realizable load impedance. The dashed circle shows the effect of a high-Q cavity connected as in Fig. 7. (L_S = 0.28 nH, L_M = 0.22 nH, C_p = 0.49 pF, C_M = 0.1 pF, f_a = 6.7 GHz, C_T = 0.44 pF, τ = 45 pS, x_d = 0.83.)

1) It should produce single-frequency operation as an oscillator or amplifier at frequency f_p;

2) It should be stable against bias-circuit oscillations at low frequencies;

3) It should be stable against parametric oscillations from low frequencies up to the vicinity of f_p at any drive level.

These requirements clearly cover the whole frequency band from dc up to f_p, thus calling for a very broad-band design of $Z_L(f)$.

Requirement 1 determines the necessary value of the load impedance at the operating frequency $Z_L(f_p)$. For an amplifier the load impedance should be in the vicinity of the negative diode impedance as shown in Fig. 4. In the case of a high-Q oscillator a resonance loop is also superimposed upon $Z_L(f)$ which will change the load impedance to match the negative diode impedance at the desired operating frequency and power level.

Design details for requirement 2 are covered in [1]. Generally, a load impedance with a high resistive component is required up to a few hundred MHz. For the illustrative example of Fig. 4, a dc resistance of 50 Ω is selected. This appears at the center of the Smith chart.

In order to satisfy requirement 3 at the subharmonic frequency $f_p/2$ condition (6) has to be met. To see the constraints imposed upon $Z_L(f_p/2)$ by (6), let us first consider equation (2). This is a bilinear transformation between S_n and Z_X. The external impedance can be expressed from (2) as

$$Z_X = -Z_W + \left(\frac{r}{1 + r - S_n}\right)\left(Z_W + j\frac{1}{\omega C_T}\right) \tag{7}$$

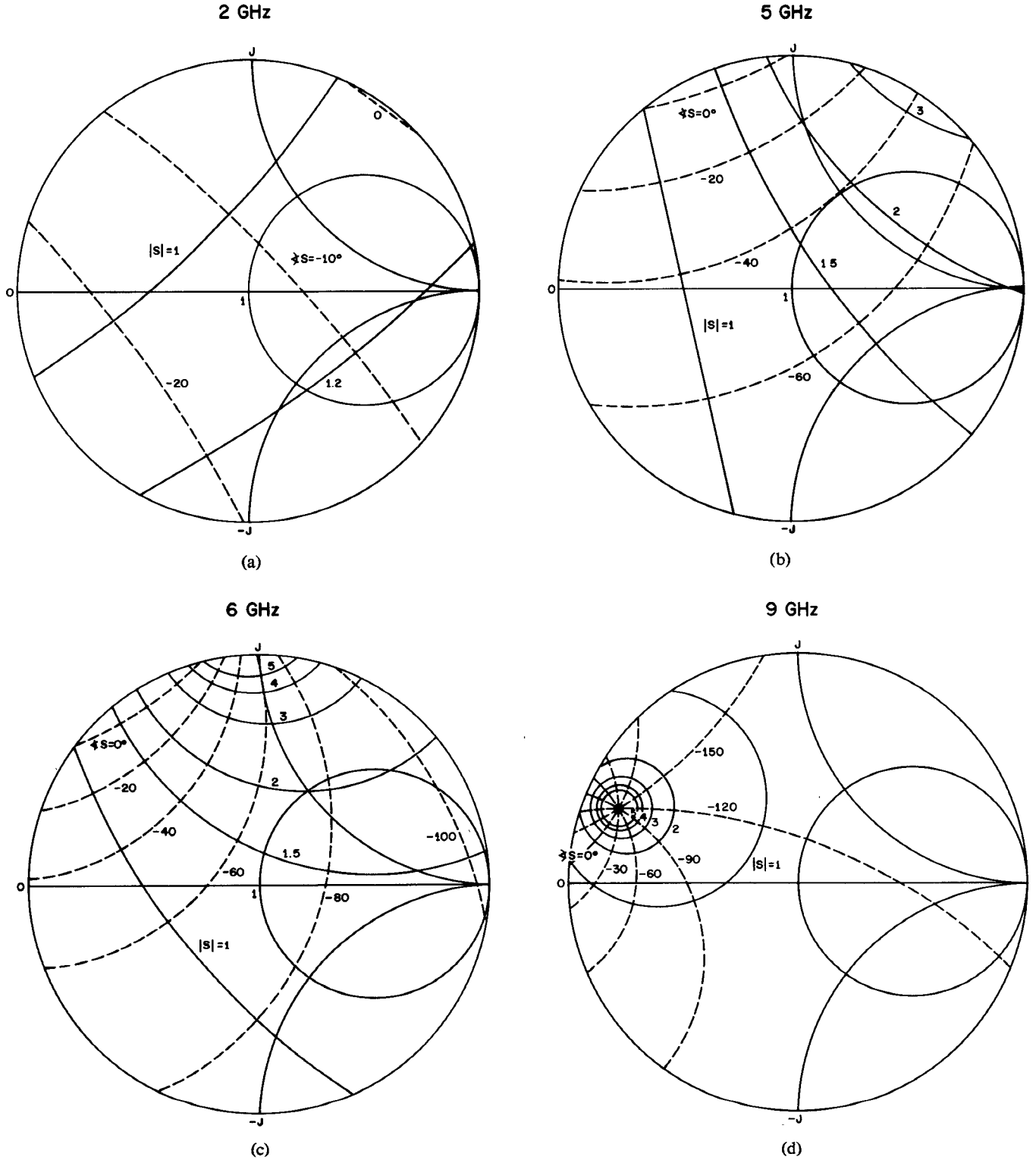

Fig. 5. Stability contours mapped on the load impedance plane. (a) 2 GHz. (b) 5 GHz. (c) 6 GHz. (d) 9 GHz.

where

$$r = \frac{(\omega/\omega_a)^2}{1 - (\omega/\omega_a)^2}.$$

Another bilinear transformation exists between Z_X and Z_L. If the diode package and mount are characterized by two-port impedance parameters, this transformation is

$$Z_L = -Z_{22} + \frac{Z_{12}Z_{21}}{Z_{11} - Z_X}. \tag{8}$$

Using (7) and (8), the trace of the $|S| = 1$ curve can be found on the Z_L plane, and the region where $|S| < 1$ can be identified (region left of the broken line in Fig. 4).

In order to partially satisfy requirement 3, i.e., to avoid parametric oscillations at the subharmonic frequency $f_p/2$, the load impedance $Z_L(f_p/2)$ has to fall within this region.

The necessary value of $Z_L(f)$ is given then (at least approximately) at three distinct frequencies: $0, f_p/2$, and f_p.

In order to make $Z_L(f)$ realizable, these three points should be interconnected with a clockwise running curve, as shown in Fig. 4.

This curve, of course, should also be shaped such as to satisfy requirement 3 for parametric stability at all the other frequencies. In the process of shaping $Z_L(f)$ it must be recalled that each point of the stability curve in Fig. 2 is determined by two stability factors, S_0 and S_{-1}. These in turn are determined by two load impedance values, $Z_L(f_0)$ and $Z_L(f_{-1})$. The allowable regions for Z_L at different frequencies are, therefore, interrelated.

A useful tool for stability analysis—as a first step—can be developed by mapping constant phase and magnitude contours of S_n onto the Z_L plane, by using (7) and (8). Computer-generated contours of this kind are shown in Fig. 5(a)–(d), calculated for 2, 5, 6, and 9 GHz, for the diode and package considered in Fig. 4, as an example. Only those contours are shown which fall into the interior of the Smith chart. In an actual design it would be useful to have additional charts for intermediate frequencies, but these four suffice for discussion.

These charts show that the phase and magnitude of S_n change very little at low frequencies, e.g., $f \leq 2$ GHz. The phase is practically always negative and the magnitude is close to one. With increasing frequency (2–5 GHz) the phase is still negative but has a much wider range and the magnitude can also be much larger than one. Above 6.7 GHz there is a singularity of $S_n(f)$, which occurs when $Z_L = -Z_D$; therefore, both the phase and magnitude of S_n become very sensitive functions of Z_L.

To analyze stability for a given $Z_L(f)$, take the two corresponding points $Z_L(f_0)$ and $Z_L(f_{-1})$ and read the values of S_0 and S_{-1} from charts like those in Fig. 5. By doing this at a number of discrete frequencies the whole $S_0S_{-1}^*$ stability curve with frequency as parameter can be constructed.

In the process of finding a stable circuit, one may consider a variety of topological forms, calculate $Z_L(f)$ for each circuit, and quickly generate the associated stability curves. At frequencies where parametric instability is indicated, it is readily apparent what change needs to be made to the load impedance to alter the phase or magnitude of S at the troublesome frequency. A few general guidelines may be stated as follows.

1) The load impedance in the frequency range much below the subharmonic, e.g., $f \leq 2$ GHz in Fig. 5, is not critical. Thus it can be chosen to satisfy Brackett's criterion [1].

2) Near the subharmonic frequency, 5–6 GHz, the behavior of the load impedance is critical, since $S_0S_{-1}^*$ is near the real axis. The load impedance should change very slowly in this frequency band (low-Q circuit).

3) Away from f_p but in the frequency range where the device conductance is negative, Z_L must not be too near $-Z_D$. This is because S varies rapidly in magnitude and phase near the singularity.

Using the approach described above, we found that load impedance characteristics which start at 50 Ω or higher (on the Smith chart) at dc, go into the capacitive region with increasing frequency, and finally approach the diode impedance at the operating frequency are the most promising for stability.

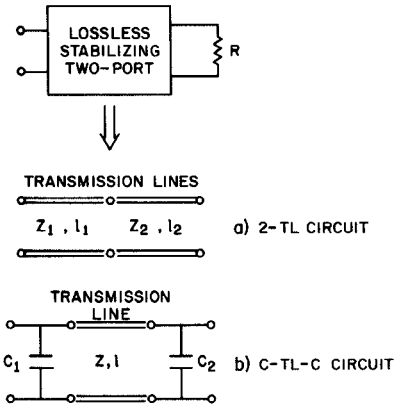

Fig. 6. General form of a stabilizing network and two circuit forms with good parametric stability.

To avoid unnecessary circuit losses, it is desirable to realize these characteristics using a lossless two port terminated by the useful load. For the lossless two port, stepped-impedance transformer-like networks have been found to approximate the desired load impedance characteristics in most cases. Two such circuits are shown in Fig. 6. The first, designated 2-TL, consists of two lengths of transmission line, which usually have low characteristic impedance and $l \leq \lambda/4$ at f_p. The second, designated C-TL-C, consists of two lumped capacitors and an intervening length of transmission line. The capacitors in the second circuit can be realized as short sections of a low-impedance transmission line.

After the desired network topology is found, the stability of the circuit can be analyzed with the help of any general network analysis computer program (to calculate $Z_L(f)$) with the addition of a subroutine to calculate the stability curve $S_0S_{-1}^*$ versus frequency using (2) and (8). The parameters of the stabilizing network then can be changed either interactively by the designer to get the desired result, or the design can be completed in a closed loop using an optimization program, which with a properly defined error function will change the network parameters until the desired response is found.

We have used both approaches successfully. For the optimization program, a desired phase and amplitude margin was specified and the error defined as the difference between these margins and the phase and magnitude of the calculated $S_0S_{-1}^*$ stability factor. This error was calculated for all frequencies up to almost f_p. At the pump frequency the error was redefined as the difference between a desired load impedance and the calculated one. The criterion function for the optimization was the weighted sum of the squared errors calculated for all frequencies.

The final result should be checked for the possibility of an undesired free-running oscillation occurring in the negative-resistance band of the diode. The stability plot may appear to predict good parametric stability in such a case. The reason is that the theory assumes the diode is driven strongly

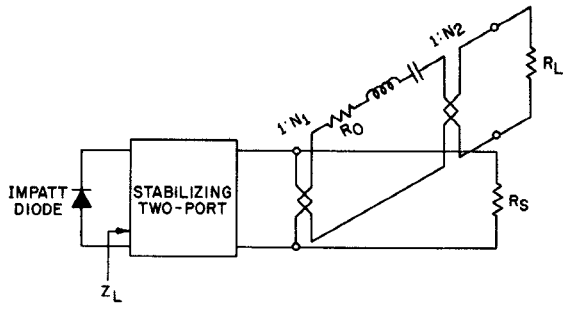

Fig. 7. High-Q oscillator circuit with a parametric stabilizing network.

at a single frequency, the pump frequency, and possibly its harmonics; if the circuit permits the diode to oscillate at a frequency other than the assumed pump frequency, the stability diagram is not valid. The stability diagram often gives warning of this situation. If the circuit matches the diode small-signal admittance at some frequency, the stability factor becomes infinite. If the circuit matches the diode large-signal admittance at some undesired frequency, the stability diagram usually rotates counterclockwise with increasing f_0.

Using the approach described above, several stable circuits have been designed for free-running oscillator and amplifier applications using a variety of diode package combinations. These results are described next. In the discussion specific diode cases are treated and corresponding values are given for the stabilizing network elements. In a more general sense, the networks to be described are prototypes which, with straightforward scaling of the frequency and impedance levels, can be used to stabilize any flat-profile GaAs diode with comparable values of the normalized avalanche and operating frequencies, $\omega_a\tau_d$ and $\omega_p\tau_d$, respectively. The scaling rules are given elsewhere [3].

B. High-Q Oscillator

In order to achieve good frequency stability, a high-Q transmission cavity is used in the free-running oscillator circuit, as shown schematically in Fig. 7. This circuit, without the stabilizing two-port, has been proposed for IMPATT oscillators by Harkless [11].

For high-Q oscillators the resonator bandwidth is quite small, often only a few MHz. Therefore, in the frequency range from dc up to "almost" f_p, the stabilizing two port is terminated by R_s. As far as the stabilizing two port is concerned, then, the circuit has the general form shown in Fig. 6.

At the desired oscillator frequency f_p the useful load R_L and the cavity losses R_0 are coupled in, and the total output power of the diode is divided between, the three resistors. There is a tradeoff between circuit efficiency and frequency stability, with the result that a high degree of frequency stability is usually associated with a sizable power loss in the oscillator circuit. Without going into quantitative analysis of the oscillator circuit, which is beyond the scope of this paper, it is clear at this point that the presence of the high-Q cavity affects the impedance transformation that the stabilizing network has to produce in order to match the diode negative impedance at f_p. The required location in the Smith chart of the impedance $Z_L(f_p)$ is then both diode and cavity dependent. For illustration, a typical impedance locus with the high-Q resonator loop is shown in Fig. 4.

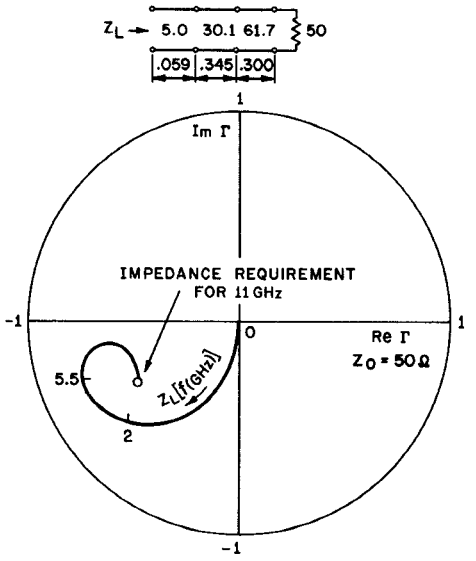

Fig. 8. An unconditionally stable circuit. Circuit schematic and impedance locus on the reflection coefficient plane.

Several stabilizing circuits have been developed for three different diode-package combinations. The results are described briefly in the following.

An unconditionally stable circuit has been developed for a GaAs diode with $V_B \simeq 50$ V, C at $V_B - 2$ V $\simeq 0.5$ pF, and $P_{dc} = 5$ W. The diode wafer has been characterized by its measured small-signal conductance and susceptance characteristics versus frequency. A curve-fitting computer program [9] was used to extract Read diode model parameters from the measured data. The diode was mounted in a standard package. The diode and package parameters were given in Fig. 4. The load impedance Z_L at $f_p = 11$ GHz was specified, from analysis of the oscillator circuit not described here, as

$$Z_L = 14 - j14\ \Omega. \tag{9}$$

Starting with a three-section maximally flat quarter-wave impedance transformer,[1] an optimization computer program produced the three-section transformer shown in Fig. 8 with the impedance characteristics shown in the same figure and the stability curve shown in Fig. 9.

This circuit satisfies all the requirements. The impedance at 11 GHz is at the desired point on the Smith chart in Fig. 8. The circuit is stable for any drive level as the stability curve of Fig. 9 indicates. The magnitude of the stability curve at $f_p/2 = 5.5$ GHz is 0.87, and there is a 33° phase margin. Also shown in Fig. 9 are curves for lower values of the avalanche frequency, corresponding to smaller values of bias power. These demonstrate that the stability improves as the bias power decreases.

[1] The use of maximally flat quarter-wave impedance transformers was suggested by A. J. Giger.

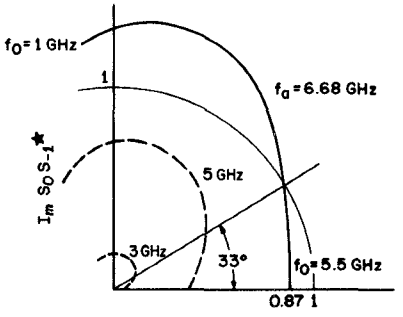

Fig. 9. Stability curve for the circuit of Fig. 8.

SUMMARY OF RESULTS FOR HIGH Q OSCILLATOR

DIODE	PACKAGE	CIRCUIT	A_m	ϕ_m
.5pF	MINI	Z_0: 9.39 26.8 50 L: .294 .304	.96	∞
.5pF	STANDARD	.85pF .65pF Z_0: 50 50 L: .155	.99	5°
		Z_0: 6 27.3 50 L: .086 .397	.83	30°
		Z_0: 5.05 30.1 61.7 50 L: .059 .345 .299	.87	33°
1pF	STANDARD	Z_0: 5 31.16 73.53 50 L: .062 .370 .165	1.19	—

Z_0 IS IN OHMS, L IS IN INCHES

Fig. 10. Stabilizing circuits developed for different diode package combinations.

Judging from the simplicity of the circuit in Fig. 8, it might appear that design of a stable circuit does not require much care. This is not the case. Two examples of simple circuits which are not stable may illuminate this point. A single section of transmission line, approximately $0.15\lambda_p$ long, transforms 50 Ω to the desired impedance at 11 GHz. However, the subharmonic impedance is then equal to $29 - j20$ Ω, which is not unconditionally stable (see Fig. 5(b) and (c)). The potential subharmonic instability may be "fixed" by placing an open-circuited stub $\lambda_p/2$ long in shunt at the load reference plane; this shorts the subharmonic without affecting the impedance at the pump frequency. However, analysis of this circuit predicts a parametric pair at 4.2 and 6.8 GHz, with a somewhat lower degree of stability than for the original subharmonic. Indeed, we have observed this effect in experiments with stubs.

Two more stable circuits have been developed for the 0.5-pF diode standard package combination. These are shown in the middle section of Fig. 10. One of them is a two-section impedance transformer (2-TL circuit) which yields almost as good stability as the three-section transformer. The second circuit consists of two lumped capacitors and a 50-Ω transmission line between them. This C-TL-C

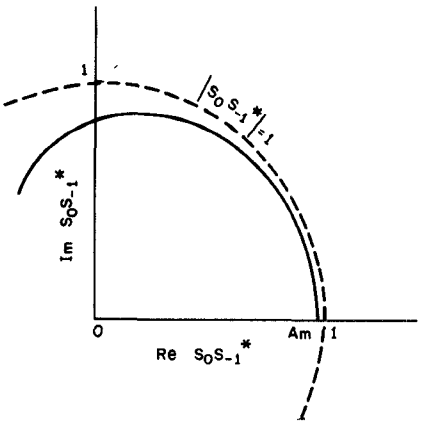

Fig. 11. Stability curve for the circuit shown at the top of Fig. 10.

circuit is also unconditionally stable, although it does not have as much margin against parametric oscillation as the other two.

A circuit has been developed for the 0.5-pF diode wafer placed into a miniature package with smaller parasitics: $L_S = 0.02$ nH, $L_M = 0.09$ nH, $C_p = 0.2$ pF, $C_M = 0.1$ pF. The two-section-transformer circuit shown at the top of Fig. 10 is stable; it has in fact infinite phase margin, i.e., it meets the strict criteria for stability [3], as shown in Fig. 11.

A limited effort was made to develop a circuit for a larger area ($C_T \simeq 1$ pF) diode in the standard package. The larger capacitance makes this diode more difficult to stabilize since, in general, parametric stability requires that the circuit impedance be low relative to the diode impedance. The best result is shown in the last row of Fig. 10. This is not a stable circuit for large-signal levels. The magnitude of the stability curve is 1.19 at the intersection with the real axis. Although this might be good enough for a medium-power amplifier or oscillator, the signal level where parametric tones are produced would probably strongly depend on the individual diode parameters.

Two of the circuits shown in Fig. 10 have been built into a high-Q oscillator and have been tested experimentally. These two were the two-capacitor circuit and the two-section-transformer circuit designed for the 0.5-pF diode in the standard package. Both circuits were found to be unconditionally stable.

The output power of the oscillator was recorded versus dc diode current for different load values as shown in Fig. 12. The monotonic shape of the measured saturation characteristics indicates that there is no oscillation at other frequencies. This has been confirmed by a spectrum analyzer coupled into the low-Q coaxial circuit. No trace of spurious tones or increased noise sidebands was found anywhere on the saturation characteristics of Fig. 12.

C. Low-Q Amplifier

The objective is to design an amplifier to be used as a test circuit for evaluating high-power 11-GHz diodes. It is desirable that the instantaneous bandwidth of the test circuit be relatively large, so that a diode may be evaluated over a range of frequencies without retuning the circuit. This means

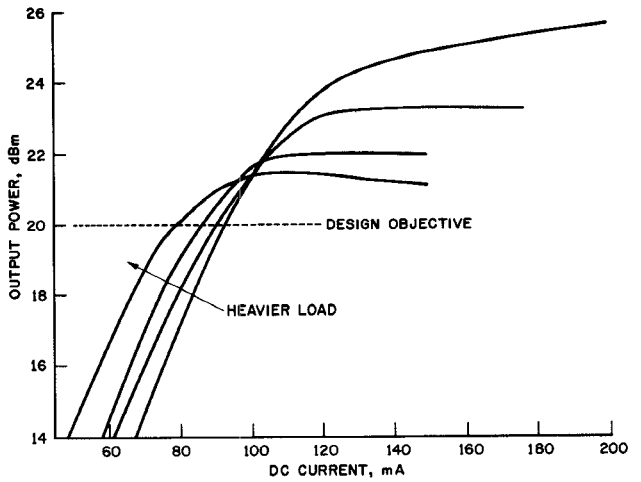

Fig. 12. Measured saturation characteristics of a stable IMPATT oscillator. (Due to losses in the high-Q cavity and the stabilizing resistor, the power generated by the diode is about 6 dB higher than shown here.)

that the circuit impedance must be near to the negative diode impedance over a range of frequencies. This constraint makes the realization of a stable circuit somewhat more difficult than for a high-Q circuit.

The nominal diode for which the test circuit is designed is a GaAs Schottky-barrier single-drift uniformly doped diode. The breakdown voltage is equal to 52.5 V, and the room-temperature junction capacitance (at 2 V less than breakdown) is equal to 1.06 pF. The capacitance is twice as large as the cases for which an unconditionally stable oscillator was designed. Fig. 13 shows the negative of the wafer impedance, transformed through the package and mount.

As before, the load impedance is constrained at the nominal pump frequency, 11.2 GHz. The circuit reactance is chosen so as to resonate the diode small-signal impedance at 11.2 GHz; the resistance, to give a gain of 20 dB; this gives $Z_L = 8.5 - j14\ \Omega$. Based on the theoretical large-signal diode admittance, the gain should decrease to about 7.5 dB when the added power is equal to 33 dBm.

The topological form of Z_L considered here is the C-TL-C circuit of Fig. 6. The impedance of the optimum circuit is shown in Fig. 13; the element values are given in the inset. There is no intersection of the load and diode curves at a common frequency, so there is no free-running oscillation. As required, the curves nearly intersect at 11.2 GHz. The circuit impedance is low and slowly varying so that the stability factor has a small magnitude and a slowly varying phase. The external Q,Q_x, computed by the formula

$$Q_X = \frac{\omega_0}{2G_X} \frac{dB_X}{d\omega}\bigg|_{\omega_0}$$

where

$$G_X + jB_X \triangleq Z_X^{-1}$$

is equal to minus one at 11.2 GHz. The sign is negative because the susceptance actually decreases slightly with frequency.

The stability diagram for this optimum case is shown in Fig. 14. The curve intersects the real axis at a value of 1.08 at the subharmonic frequency, and this is the only intersection. The interpretation of Fig. 14 is that the circuit is stable for all normalized RF pump levels, M_1, up to $M_1 = (1.08)^{-1/2} = 0.96$. As mentioned earlier, the maximum output power of the diode is expected to correspond to $M_1 \simeq 0.8$; therefore, the circuit is theoretically stable from small signals up to and beyond RF saturation.

The stabilizing circuit was realized in a 50-Ω 7-mm coaxial air line with disks on the center conductor to approximate the lumped capacitors. The broad-band 50-Ω load was realized with a complementary high-pass low-pass filter (diplexer), having a crossover frequency of 8 GHz. A circulator which is well matched from 7 to 12.4 GHz was connected to the high-frequency port of the diplexer, to separate the incident and reflected waves at the test frequency. The low-frequency port of the diplexer was connected to a dummy load, through a bias tee. The power added by the diode is computed, taking into account the small losses in the circulator, diplexer, and stabilizing circuit. The diode large-signal admittance may be evaluated by measuring both the amplitude and phase of the incident and reflected waves [10]. The output spectrum of the diode is routinely checked from 100 MHz to 14 GHz.

The crossover frequency of the bias tee was measured to be about 100 MHz. Below this frequency the bias stabilization network, a passive lumped *RLC* circuit, designed to provide a high impedance, is coupled to the diode. In all testing to date, no bias circuit oscillations have been observed.

A typical curve for the saturated output power, measured with the dc power held constant at 19 W and the diode case temperature equal to 60°C, is given in Fig. 15. Data were taken at 100-MHz intervals from 9 to 12 GHz. At each frequency the input level was varied so that the added power increased, reached a peak, and then decreased with further increases in the input power level. During this operation the output spectrum was monitored continuously; no spurious tones were observed. The scatter in the data is attributed to mismatch errors in determining the incident and reflected power, which are magnified when computing added power.

It is noteworthy that no spurious tones appeared, as the pump frequency was varied from 9 to 12 GHz. The stabilizing circuit was designed considering only one pump frequency, 11.2 GHz. The independence of the stability from the pump frequency is due to the slowly varying circuit impedance, which leads to a simple shape for the stability diagram.

The test circuit was designed for a diode with nominal parameters. It is important to determine how the stability is affected by variations in the diode parameters. To date, more than 100 diodes have been tested in the circuit, with breakdown voltages ranging from 45 to 55 V and junction capacitances ranging from 0.9 to 1.1 pF. Insofar as possible, diodes have been selected from all parts of this "window," to evaluate the circuit fully. Approximately 80 percent of

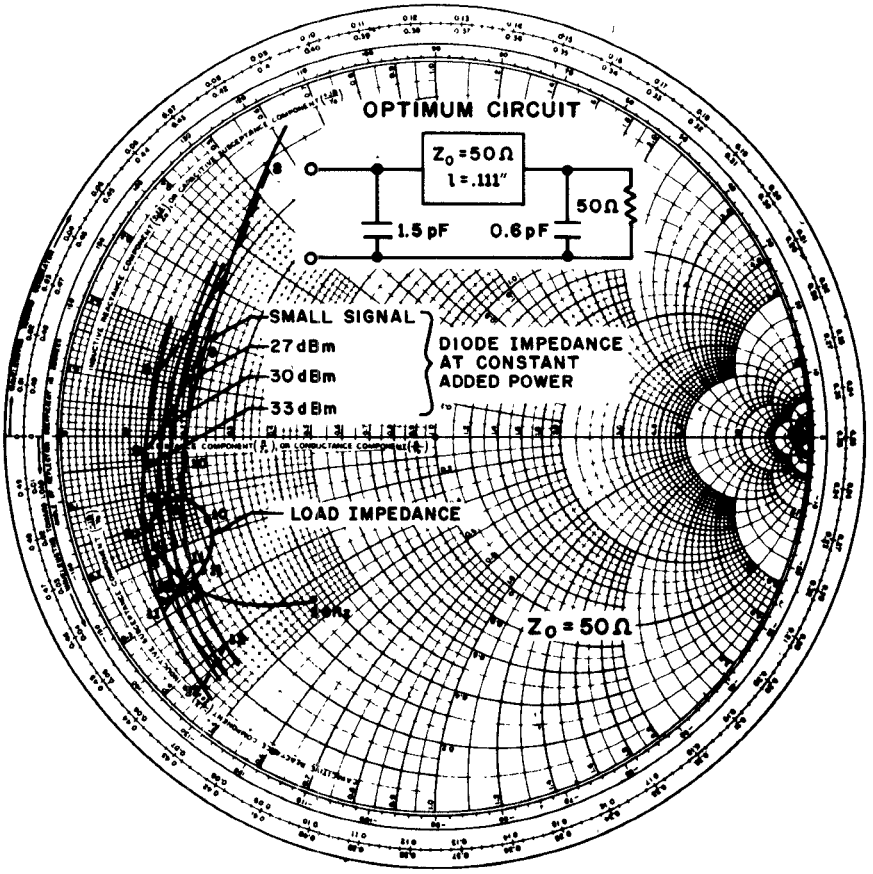

Fig. 13. Circuit impedance and negative of the nominal diode impedance. (L_S = 0.27 nH, L_M = 0.2 nH, = 0.44 pF, C_p $C_M = 0$, f_a = 7.7 GHz, C_T = 0.84 pF at operating temperature, τ_d = 45 pS, x_d = 0.85.)

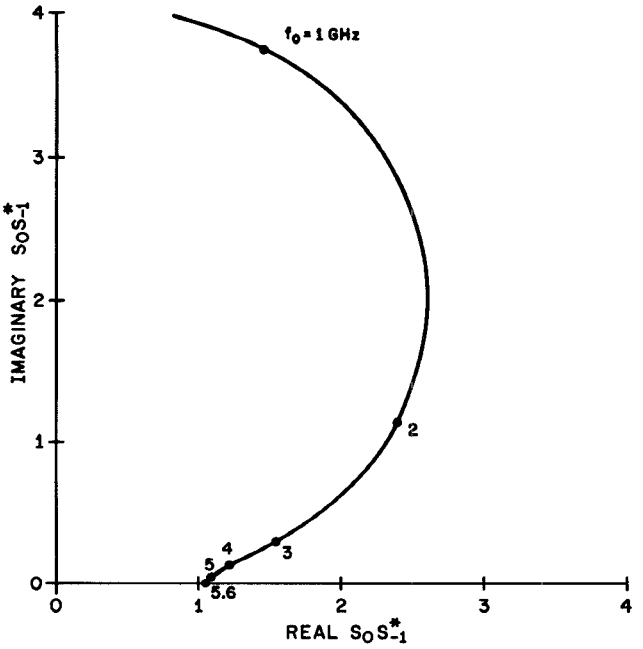

Fig. 14. Stability diagram for the optimum circuit, for a pump frequency of 11.2 GHz.

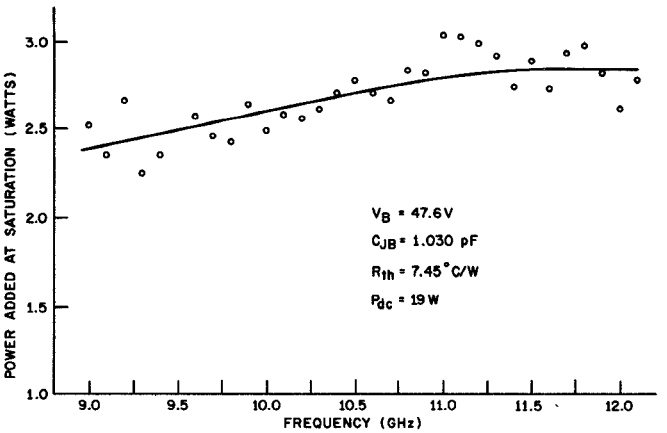

Fig. 15. Saturated output power of a typical IMPATT diode.

the diodes were tested satisfactorily on the first try. That is, when placed in the fixed-tuned circuit they could be driven to power saturation with no spurious tones appearing. The remaining 20 percent did display parametric-pair tones a little below saturation, usually at about 3.5 and 7.7 GHz. However, it was always possible to retune the circuit, using a capacitive-screw trimmer, to suppress the spurious oscillations and permit the diode to be driven to saturation. All diodes could be fully characterized. No subharmonic oscillation was ever observed.

IV. Conclusions

A method has been described for applying the theory of parametric interactions in IMPATT diodes to the design of practical circuits which suppress such spurious oscillations. The method permits one to consider a much wider range of circuits than those which satisfy the sufficiency criteria suggested earlier [3].

The diode is characterized by four Read model parameters. The package parasitics are included in the formulation of the requirements for the load.

Using the methods outlined in this paper, several oscillator circuits, which indicate unconditional stability against parametric effects, have been developed for different diode package combinations. Two of these circuits were built and tested in a laboratory model of an 11-GHz IMPATT diode oscillator. Neither has shown any sign of the "secondary effects," listed in the introduction, even when driven into full saturation.

Also, a conditionally stable amplifier, which is used as a test circuit for high-power 11-GHz IMPATT diodes, has been designed and built. For a wide range of diode parameters and test frequencies the diode can be driven to power saturation without the occurrence of spurious tones.

The stabilizing circuits described can be directly applied to similar IMPATT diodes by appropriate scaling.

The networks considered here are, ideally, lossless. In practical cases there is some loss, the degree of which depends upon the physical realization. In an amplifier designed for low-cost manufacture, the loss could be typically of the order of 1 dB. Since the stabilizing network is interposed between the diode and the external load, the maximum available power is somewhat less than the maximum diode power.

A manufacturable amplifier (or oscillator) requires tuning adjustments to effect a nominal gain (or power output) for a range of diode parameters. Such adjustments may cause a significant change in the out-of-band circuit impedances, which can seriously affect the stability against parametric oscillations. Although this is a more complex problem, the techniques presented here can be used to design a circuit which gives the best compromise between the stability and tuning range.

Acknowledgment

The support of R. P. Snicer and E. D. Walsh in developing the computer programs is gratefully acknowledged. W. J. Love assisted in fabricating the amplifier circuit and performed most of the diode evaluations. The authors are grateful to J. W. Gewartowski, A. J. Giger, and R. E. Sherman for valuable comments and suggestions.

References

[1] C. A. Brackett, "The elimination of tuning-induced burnout and bias-circuit oscillations in IMPATT oscillators," *BSTJ*, vol. 52, no. 3, pp. 271–306, Mar. 1973.
[2] M. E. Hines, "Large-signal noise, frequency-conversion and parametric instabilities in IMPATT diode networks," *Proc. IEEE*, vol. 60, pp. 1534–1548, Dec. 1972.
[3] W. E. Schroeder, "Spurious parametric oscillations in IMPATT diode circuits," *BSTJ*, vol 53, no. 7, pp. 1187–1210, Sept. 1974.
[4] J. J. Goedbloed and H. Tjassens, "Parasitic oscillations in IMPATT-diode oscillators," in *Proc. 4th European Microwave Conf.* (Montreux, Sept. 1974), pp. 328–332.
[5] J. J. Goedbloed, "Investigations of parasitic oscillations in IMPATT-diode oscillators by a simple locus chart," *Electron. Lett.*, vol. 11, no. 3, pp. 54–56, Feb. 6, 1975.
[6] D. F. Peterson, "Circuit conditions to prevent second-subharmonic power extraction in periodically driven IMPATT diode networks," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 784–790, Aug. 1974.
[7] R. L. Kuvås, private communication.
[8] W. T. Read, Jr., "A proposed high-frequency negative resistance diode," *BSTJ*, vol. 37, pp. 401–446, Mar. 1958.
[9] Y. L. Kuo, "Modeling of IMPATT diodes for circuit and noise analysis," presented at the 1975 IEEE Int. Symp. Circuits and Systems, Newton, MA, Apr. 1975.
[10] D. R. Decker, C. N. Dunn, and R. L. Frank, "Large-signal silicon and germanium avalanche-diode characterization," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 872–876, Nov. 1970.
[11] E. T. Harkless, U.S. Patent 3 534 293, Oct. 30, 1970.